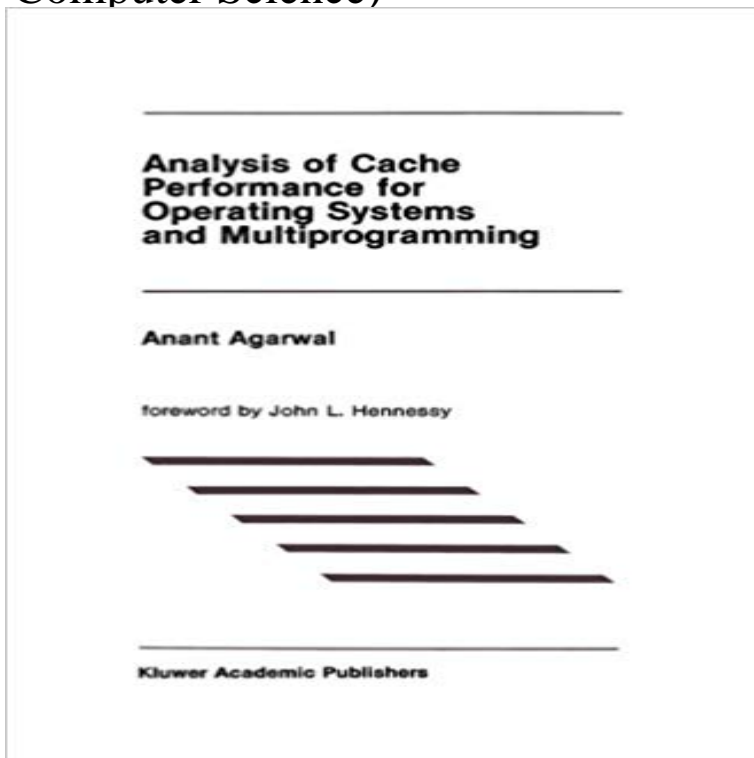


Analysis of Cache Performance for Operating Systems and Multiprogramming (The Springer International Series in Engineering and Computer Science)



As we continue to build faster and faster computers, their performance is becoming increasingly dependent on the memory hierarchy. Both the clock speed of the machine and its throughput per clock depend heavily on the memory hierarchy. The time to complete a cache access is often the factor that determines the cycle time. The effectiveness of the hierarchy in keeping the average cost of a reference down has a major impact on how close the sustained performance is to the peak performance. Small changes in the performance of the memory hierarchy cause large changes in overall system performance. The strong growth of microprocessors, whose performance is more tightly coupled to the memory hierarchy, has created increasing demand for high performance memory systems. This trend is likely to accelerate: the improvements in main memory performance will be small compared to the improvements in processor performance. This difference will lead to an increasing gap between processor cycle time and main memory access time. This gap must be closed by improving the memory hierarchy. Computer architects have attacked this gap by designing machines with cache sizes an order of magnitude larger than those appearing five years ago. Microprocessor-based RISC systems now have caches that rival the size of those in mainframes and supercomputers.

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