Multi-core and Many-core Computers: Dataflow Parallelism in Teradevice Computing

This book provides the most up-to-date overview of EU-funded research on Multi- and Many-core Computing Systems. Several relevant projects are considered, each of them providing a unique integrated or focused team involving leading European Universities, Institutions and Industries that attack the challenges and provide different solutions to realize future computers.

Architectural Support for Fault Tolerance in a Teradevice Dataflow In the Journal of Parallel and Distributed Computing, October 2012. with Data-Flow Languages Multi-Core and Reconfigurable Super Computing Conference, Many-core and Reconfigurable Super Computing Conference, Belfast, 2008. I was awarded the Hoare Prize for the highest 1st in Computer Science that year. **TERAFLUX: Exploiting Tera-device Computing - Semantic Scholar** I/O Buses (PCIe, USB, Ethernet, SATA HD) PCIe. PCIe. On Chip core. L1 Inst L1 Data Multi-core Chip. M e m o ry Computer. Cores. Rmax. Rpeak. Power Mflops/Watt. 1 Tianhe-2 . in Teradevice Computing. TeraFlux. Multithreading+dataflow to exploit the high parallelism in future many-core devices (1000+ cores). **Future Generation Computer Systems A scalable thread scheduling** L. Verdoscia, R. Giorgi, A Data-Flow Soft-Core Processor for Accelerating Scientific a Teradevice Dataflow System, Springer Int.l Journal of Parallel Programming, New York, Tera-device Computing Challenges, ELSEVIER Procedia Computer Single-Chip Multicore Architectures, Journal of Embedded Computing, **Toward a Self-Aware Codelet Execution Model** Founder and leader of the Computer Architectures and Parallel Systems Participated in the MIT Static Dataflow Architecture Project and other projects . Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG08, 09, 10, . Toward High Performance and Energy Efficiency on Manycore Architectures **Roberto Giorgi** Many-core, multi-core, dataflow. 1. INTRODUCTION. Data-flow computing is a well known paradigm that is capable of taking advantage of the full parallelism **A Scalable Distributed Data-flow Scheduler for Many-Cores none** forecasts predict that future parallel computing systems may contain more than 1,000 ther raise [43], making faults in present multi-core and future

many-core systems In: International Symposium on Computer Architecture and High **Enhancing an x86_64 Multi-Core Architecture with - AXIOM Project** Future Generation Computer Systems archive . explored in order to exploit the high parallelism offered by future massive many-core chips. We propose a minimalistic core ISA extension for data-flow threads. . Detection and Recovery Architecture for a Teradevice Dataflow System, Proceedings of the Multi-core and Many-core Computers: Dataflow Parallelism in Teradevice Computing at - ISBN 10: 1461414830 - ISBN 13: 9781461414834 **View - AXIOM Project** BSc (2006-2010): Computer Science, University of Cyprus, Cyprus o PhD Internship in Many-core Software Development using the Flexaware Platform o EU FP7 Project TERAFLUX: Exploiting Dataflow Parallelism in Teradevice Computing into the Data-Driven Multi-threading Model using the TFlux Platform, **The TERAFLUX Project: Exploiting the DataFlow Paradigm - CAPSL OmpSs: A PROPOSAL FOR PROGRAMMING HETEROGENEOUS** support thread scheduling in the architecture on a many-core chip. larger than current multi-core systems. scheduling threads among the computing resources is not a trivial problem [AP12]. . TERAFLUX: exploiting dataflow parallelism in teradevices. In Computer Architecture and High Performance Computing,. **A scalable thread scheduling co-processor based on data-flow** Teradevice Dataflow System. Sebastian doors for new highly scalable computing systems with prob- ably more than further raise [30], making faults in present multi-core and fu- the number of cores and the increasing failure probability on a chip in fault-tolerant architecture for a parallel and hierarchically threaded **State-of-the-art Computing Systems Typical Multi-core Structure** Procedia Computer Science 7 (2011) 146147. The European Future Keywords: Tera-device Many-core Parallelism Reliability Dataflow. 1. Overview of the **TERAFLUX: exploiting dataflow parallelism in teradevices** According to semiconductor roadmaps, future computing. Keywords. Tera-device Many-core Parallelism Reliability Dataflow **Download my CV - Andreas Diavastos** He received his PhD in Computer Engineering and his MS in Electronics Engineering, . of multi-core multi-board systems through the open-source OmpSs Architectures and Tools for Many-Core systems Future Teradevice Systems, i.e. . Dataflow Parallelism in Teradevice Computing in cooperation with University of **Docs - CAPSL - University of Delaware** Department of Electrical and Computer Engineering The Codelet Model is a fine-grain dataflow-inspired and event- parallel programs on a combination of such many-core chips into . Grain Dataflow Multi-Threading: Codelets themselves can . Harnessing dataflow in next generation teradevices, Microprocessors. **TERAFLUX: Harnessing dataflow in next generation teradevices** Task-parallel programming models combining dataflow and stateful .. on Computer Architecture and High Performance Computing, 2007, A. Portero, Z. Yu, R. Giorgi, Teraflux: exploiting tera-device computing challenges, Procedia .. framework for multicore and manycore architectures, Proceedings of **Exploiting dataflow parallelism in Teradevice Computing - Cordis** d INRIA, France e Dept. of Computer Science, University of Cyprus, Nicosia, Cyprus .. ture consists of a number of multi-core nodes. We are ISA agnostic,. **Publications TERAFLUX** A Dynamic Schema to increase performance in Many-core Architectures through COStream: A Dataflow Programming Language and Compiler for Multi-core . Roberto Giorgi, TERAFLUX: Exploiting Dataflow Parallelism in Teradevices, A compiler and runtime system perspective to scalable data-flow computing. **Roberto Giorgis Papers** future computer systems. New silicon parallelism which emerges in future teradevices. . The basic architecture consists of a number of multi-core nodes. **TERAFLUX - ACM Digital Library - Association for Computing** [2] M.D. Hill, M.R. Marty, Amdahls law in the multicore era, Computer 41 (7) Strudel, A clustered manycore processor architecture for embedded and accelerated dataflow parallelism in teradevices, in: ACM Computing Frontiers, 2012, pp. **Creativity in Computing and DataFlow SuperComputing - Google Books Result** To exploit this parallelism, threaded dataflow execution. Abstract: Future computing systems (Teradevices) will probably contain more than 1000 cores on a single die. Published in: Data-Flow Execution Models for Extreme Scale Computing parallel architectures, data flow computing, fault tolerant computing, multi- **Multi-core and Many-core Computers: Dataflow Parallelism in** Multi-core and Many-core Computers: Dataflow Parallelism in Teradevice Computing at - ISBN 10: 1461414830 - ISBN 13: 9781461414834 **Multi-Core and Many-Core Computers: Dataflow Parallelism in** Co-processor architecture. Data-flow. Many-core. High-performance systems abstract models can be explored in order to exploit the high parallelism offered by future massive many-core chips. . system is composed of a mix of multi-core, many-core chips and and Emerging Technologies for Teradevice Computing. **A Fault Detection and Recovery Architecture for a Teradevice** Multi-core and Many-core Computers Free delivery on online orders of $99.99 or Computers: Dataflow Parallelism in Teradevice Computing. **CAPSL: Publications** CF 12 Proceedings of the 9th conference on Computing Frontiers . R. Giorgi, TERAFLUX: Ideas for the Future Many-Cores, ODES: Workshop on .. parallel computers equipped with general purpose multi-core processors